DMiX

OPERATOR MANUAL

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1.0 Product Description

The LSC Lighting System's **DMiX** merge unit adds flexibility to any DMX data network. The **DMiX** is designed to operate with and complement the LSC DNA range of data processing equipment.

The **DMiX** is a two (2) input to one (1) output merge unit, capable of merging two 512 channel DMX streams into one 512 channel DMX output stream.

The **DMiX** will adequately operate as a stand-alone unit, as well as being integrated into a large DNA networked system. The following sections outline product features and technical specifications. Should more information be required, please contact your LSC distributor or LSC Lighting Systems directly. We are here to help.

1.1 Features

- Two DMX input streams. 'A' and 'B' both with loop through connectors.
- Data streams merged on HTP (Highest Takes Precedence) basis.
- 'A' stream start address internally set to 1 (no offset).
- 'B' stream start address is user settable via front panel pushbuttons and easily read 3 digit LED display. Addressing range 001 to 512.
- Output is full speed DMX512
- All inputs have green data present activity LEDs and red data error LEDs.
- 23.5 millisecond (fast) system propagation delay (input to output time).
- User altered settings are retained in memory so that the unit will power up in the exact settings that it powered down in.
- DMX input /output via 5 pin AXR style connectors.
- Will run stand-alone or connect into an LSC DNA system.
- 1 Rack Unit (1 R.U.) cabinet suitable for rack mounting.
- A power loss will automatically connect input stream 1 to output stream 1.

1.2 Technical Specifications

Digital Input RS485 differential (balanced) line on 5-pin AXR style connectors.
2 x Male AXR with Female AXR loop through.

Digital Output RS485 differential (balanced) line on 5-pin AXR style connector.
1 x Female AXR.

Digital Protocol DMX512/1990 250KBaud to USITT standards. (Refer Appendix A)

Isolation All DMX inputs and outputs are optically isolated with separate line receiver, opto-coupler and isolated power supply.

Address range 001 to 512 on second DMX stream

Propagation Delay 23.5mSec (0.0235 seconds) for any input to output.

Power consumption 30 Watts max.

Input Supply 120 / 240VAC selectable with voltage selector inside the fuse drawer of the IEC power inlet. 50/60Hz auto selectable.

Input Supply range 120VAC setting 100-130VAC
240VAC setting 200-260VAC

Dimensions 480 mm x 175 mm x 44 mm (W x D x H). 1 R.U.

Approvals CE Mark and C-Tick.

Weight 3 Kg unpacked.

2.0 DMiX Operation

The **DMiX** input stream 'A' is internally set to begin at DMX address 001. Stream 'B' is set to whatever DMX start address is required by using the associated address setting buttons. Two keys and a 3-digit LED display are dedicated to the B stream. The upper button will increment the address and the lower button will decrement the address. Addresses will change with each button press, but if the button is held down the rate of address increments/decrements will increase. This allows a new address to be reached quickly.

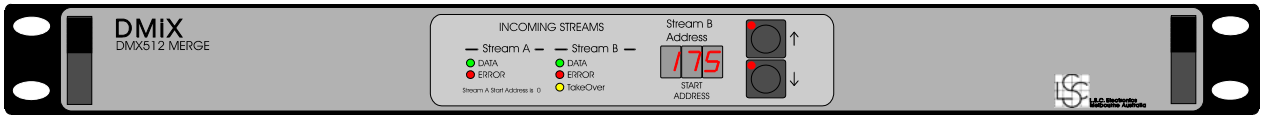
The range of 'B' stream start address is from 001 to 512. The address value will wrap around when it reaches either address 512 or 001. That is, if the display reads 512 and the increment key is pressed the address will wrap around to 001. Addresses, TakeOver status and all preset data set during operation are internally stored in memory, and are recalled on power-up so that the DMiX will wake up in the same mode of operation it was in when powered down.

All settings are internally stored <u>5 seconds after modification</u>.

The two input data streams are HTP (Highest Takes Precedence) merged to produce a single 512 channel DMX output stream. 5-pin AXR style connectors on the rear panel allow for direct connection to the DMiX data streams using USITT standard DMX cabling.

2.1 Front Panel Controls

<u>Front View of the DMiX</u>

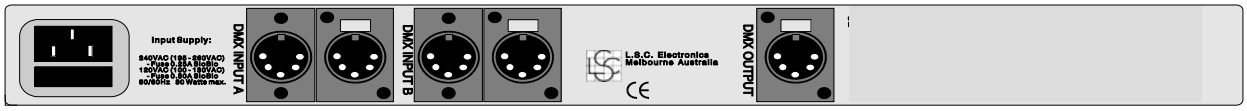


The front panel consists of two sets of "data status" LED indicators and LED address display with associated increment / decrement keys for the second input stream DMX start address.

Each input has a set of indicators featuring a green DATA LED to indicate the presence of DMX data. The second indicator is a red ERROR LED. This LED will illuminate if the DMiX receives any data errors during reception. ***If the DMiX exhibits some apparently random behaviour then check first to see if any data errors are being received***.

The DMX start addresses for the B stream is set by pressing the increment [up arrow] or decrement [down arrow] button. Pressing and holding a button will change the display one address unit at a time. After a few seconds the display will change more rapidly allowing quicker address setting.

2.2 Rear Panel Controls and Connections



Rear View of the DMiX

The rear panel of the **DMiX** features DMX input and output connectors and the mains power input connector. (Refer to the specifications section for voltages ranges). The **DMiX** will operate from either 120 or 240 VAC sources. The fuse drawer of the IEC inlet is removable and allows for selection between 120 and 240VAC operation.

Next are the DMX input AXR connectors. Each of the 2 inputs features both male and female (loop through) AXR style connector pairs. The output connector is a single female AXR style connector.

2.3 Data Stream Merging Concepts

Data stream merging is a simple concept. Because of the nature of digital data transmission, signal lines cannot simply be connected together. If this were to occur the data on each DMX line would be corrupted by the other and no intelligible data would be recoverable at the receiver. Analog systems may be connected together, using diodes, without compromising signal integrity.

In the **DMiX**, the A stream is internally set to begin at address 1. The second input has an associated address setting which will position the incoming B stream data to begin at the set address. The data streams are then “mixed” on a HTP basis to produce a final output.

2.3.1 HTP

HTP is an acronym for Highest Takes Precedence. This means that if comparing 2 (or many) values, the number which is the largest will be the one chosen. In the example below, channel 4 on the output is derived through a comparison between channel 4 of stream A (30) and channel 2 of Stream B (40) (Stream B address start is 3). The resulting value passed to the output is 40 as it is higher than 30.

50 20 30 30 90 80 10	Stream A >Internally set to begin at address 1
30 40 40 50 60 80 90	Stream B >User set to address 3 (example)

Internal operation places Streams 1 and 2 as shown.

50 20 30 30 90 80 10	Stream A
30 40 40 50 60 80 90	Stream B Merge on HTP basis.
50 20 30 40 90 80 60 80 90	Output Stream

2.4 Address Setting

Two buttons and a 3-digit LED display are dedicated to set the starting address of the B stream. The upper button will increment the address and the lower button will decrement the address. Addresses will change with each button press, but if the button is held down the count rate increases. This allows a new address to be reached quickly. Addresses will rollover from 001 to 512 when decrementing and from 512 to 001 when incrementing. The selectable address range is from 001 to 512.

Addresses, TakeOver status and all preset data set during operation are internally stored in memory and are recalled on power-up so that the **DMiX** will wake up in the same mode of operation it was in when powered down.

All settings are internally stored 5 seconds after modification.

2.5 Power Fail Conditions

Should power be lost to the **DMiX**, an internal circuit will connect DMX input stream A to output 1. This will at least allow some DMX data to pass through to the dimming equipment.

The **DMiX** features internal memory to save the **DMiX** status. ***The status will be saved five seconds after address changes, TakeOver mode changes or preset number changes***. Upon power up, the internal memory is read and the system status restored. The power off data storage time is approximately 100 years.

3.0 Appendix A: DMX512/1990 USITT Specification

1.0 SCOPE

This Standard describes a method of digital data transmission between controllers and dimmers. It covers electrical characteristics, data format, data protocol, connector type, and cable type.

2.0 APPLICABILITY

This standard is intended as a guide for:

1. Equipment manufacturers and system specifiers who wish to integrate systems of dimmers and controllers made by different manufacturers.
2. Equipment manufacturers seeking to adopt a basic controller-dimmer digital transmission protocol.

Although widespread adoption of this standard is sought by USITT, compliance with the standard is strictly voluntary. Furthermore, it is not intended as a replacement for existing protocols already manufactured, but rather as an addition to existing protocols which will broaden the installed base of controllers and dimmers that can communicate with each other.

3.0 CROSS REFERENCE

See EIA standards EIA-422A and EIA-485 available from:

Electronic Industries Association
Standards Sales Office
2001 Eye Street NW
Washington DC 20006
Ph. 202-457-4900

4.0 ELECTRICAL SPECIFICATIONS

The standard shall follow EIA Standards EIA-485 (an enhanced version of EIA-422A) with regard to all electrical characteristics including line driver and receiver selection, line loading, and multi-drop configurations.

4.1 COMMON MODE VOLTAGES

Equipment designers are advised to pay particular attention to the Common Mode voltage provision of EIA-485 in the choice of transmitter and receiver components and general system implementation.

4.2 ELECTRICAL ISOLATION

This Standard and EIA-485 make no general provisions for electrical isolation. However, suitable optical isolation, transformer isolation, or other means may be employed to prevent the undesirable propagation of voltages which exceed the Common Mode limits of EIA-485. The inclusion of such general isolation does not, however, alter the requirement that a transmitter or receiver conform to EIA-485.

5.0 DATA PROTOCOL

Data transmitted shall be in asynchronous serial format. Dimmer level data shall be transmitted sequentially beginning with dimmer 1 and ending with the last implemented dimmer, up to a maximum of 512. Prior to the first level transmitted, a RESET signal shall be transmitted followed by a NULL START code. Valid dimmer levels shall be 0 to 255 decimal (00 to FF hexadecimal) representing dimmer control input levels of OFF to FULL in a linear relationship. These numeric values shall not necessarily have any relationship to actual dimmer output, which shall be determined within the dimmer itself.

5.1 RESET SIGNAL

The RESET signal (Timing Diagram Designation #1) shall consist of a BREAK lasting 88 μSeconds (two frame times) or any longer duration. A BREAK shall be defined as a high-to-low transition followed by a low of at least 88 μSeconds. All dimmers and other receiving devices shall interpret any such BREAK as a terminator for any pending transmission/data packet and its end as the start of the MARK AFTER BREAK and START code sequence at the beginning of the next packet.

5.1.1 Mark After Break

The duration of the MARK that separates the RESET/BREAK and the START code (Timing Diagram Designation #2) shall be not less than 8 μSeconds nor greater than 1 Second. All DMX512/1990 transmitters shall produce a MARK AFTER BREAK of not less than 8 μSeconds. All receivers shall recognise a MARK AFTER BREAK of minimum 8 μSeconds. receivers also capable of recognising the shorter 4 μSeconds MARK AFTER BREAK specified in the 1986 DMX512 specification and produced by some transmitters in the field may be so identified and marked as per Paragraph 11.0

5.2 NULL START CODE

The NULL START code shall be defined as a properly framed NULL character (all zeros) following a RESET. The NULL START code is the data packet identifier which identifies subsequent data as sequential dimmer level information.

5.3 OTHER OPTIONAL START CODES

In order to provide for future expansion and flexibility in controlling devices other than dimmers, this standard makes provision for 255 additional START codes (1 through 255 decimal, 01 through FF hexadecimal). For this reason, a dimmer receiver must not accept as 8-bit level data, any data packet with a START code other than a NULL START following the RESET.

5.4 MAXIMUM NUMBER OF DIMMERS

Each data link shall support up to 512 dimmers. Multiple links shall be used where larger numbers of dimmers are required.

5.5 MINIMUM NUMBER OF DIMMERS

There shall be no minimum number of dimmers on the data link. DMX512 data packets with levels for less than 512 dimmers may be transmitted, provided that the conditions of this Standard, including Paragraphs 5.0 and 5.0.8 are observed.

5.6 DEFINED LINE BETWEEN FRAMES

The time between any two frames of a data packet (Timing Diagram Designation #8) may vary between 0 μSeconds and 1 Second. The line must remain in the "marking" state during any such idle period greater than 0 μSeconds. A receiver must be capable of accepting a data packet having no idle time (0 μSeconds) between any of its frames.

5.7 DEFINED LINE STATE BETWEEN DATA PACKETS

Regardless of START code or length, every data packet transmitted on the data link must begin with a RESET, MARK AFTER BREAK and START code sequence as defined above. The time between the second stop bit of the last data byte/frame of one data packet and the falling edge of the beginning of the RESET for the next data packet (Timing Diagram Designation #9) may vary

between 0 μSeconds and 1 Second. The line must remain in an idle ("marking") state throughout any such period greater than 0 μSeconds. Transmitters, therefore, may not produce multiple BREAKs between data packets. Receivers must, however, be capable of recovering from multiple BREAKs produced by data line errors.

5.8 MINIMUM BREAK SPACING

The period between the falling edge at the start of any one BREAK shall be not less than 1196 μ Seconds from the falling edge at the start of the next BREAK.

6.0 DATA FORMAT

The data transmission format for each level transmitted shall be as follows:

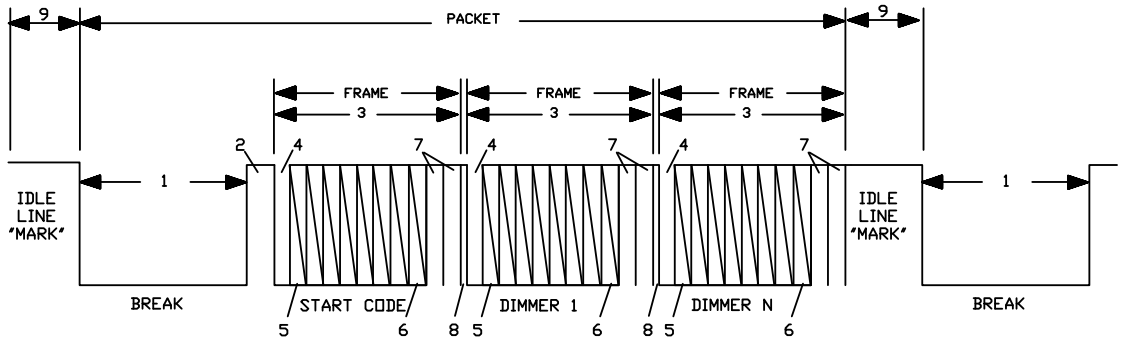
BIT POSITION	DESCRIPTION
1	Start Bit, Low or SPACE
2 -9	Dimmer level Data Bits, Least Significant Bit to Most Significant Bit, Positive Logic.
10,11	Stop bits. High or MARK
parity	Not transmitted

7.0 DATA RATE

The data rate and associated timing shall be as follows:

Data Rate:	250 Kilobits per second
Bit time:	4.0 microseconds
FRAME TIME:	44.0 MICROSECONDS
Maximum update:	22.71 milliseconds
Rate for 512 dimmers including RESET and START	4.03 times per second

7.1 TIMING DIAGRAM



DESIGNATION	DESCRIPTION	MIN	TYP	MAX	UNIT
1	"Space" for BREAK		88.00	88.00	μSEC
2	"Mark" between BREAK			8.00	μSEC
	and START code			1.00	SEC
3	Frame Time	43.12	44.00	44.88	μSEC
4	Start Bit	3.92	4.00	4.08	μSEC
5	Least Significant Data Bit	3.92	4.00	4.08	μSEC
6	Most Significant Data Bit	3.92	4.00	4.08	μSEC
7	Stop Bit	3.92	4.00	4.08	μSEC
8	"Mark" Time between Frames	0.00	0.00	1.00	SEC
9	"Mark" Time between Packets	0.00		1.00	SEC

8.0 LOSS OF DATA TOLERANCE

The receiving device must maintain, for a minimum of 1 Second, the last valid level received for each connected dimmer. Designers of transmitters are reminded that a low number of dimmer level (START CODE 00) updates may be interpreted by a receiver as loss of data.

8.1 RECEIVER DATA RATE TOLERANCE

DMX512/1990 is intended to make possible the interconnection of lighting control equipment by different manufacturers. It does not specify the minimum performance levels of connected equipment, either in terms
of the number of updates per second produced by a transmitter, or by requiring that all level updates on the data link be used by receiving product.

The performance of any product incorporating a DMX512/1990 receiver must, however, not be degraded by the presence at its input of the continuous transmission of data packets containing any number of dimmer levels up to the maximum update rates specified in Section 5 Paragraph 7.0 above.

9.0 CONNECTORS

Where connectors are used, the data link shall utilise 5-pin "XLR" style microphone connectors. Some manufacturers of this connector are:

Switchcraft
ITT Cannon
Neutrik

9.1 CONNECTOR SEX

Female connectors shall be utilised on controllers or other transmitting devices and male connectors shall be utilised on dimmers and other receiving devices. In cases where an optional second data link is implemented using the spare pins of the connector for directional transmission, female connectors shall still be utilised on the controller.

9.2 CONNECTOR PIN DESIGNATION

Connector Pin Designations shall be as follows:

PIN 1 - Signal Common (Shield)
PIN 2 - Dimmer Drive Complement (Data 1 -)
PIN 3 - Dimmer Drive True (Data 1 +)
PIN 4 - Optional Second Data Link Complement (Data 2 -)
PIN 5 - Optional Second Data Link True (Data 2 +)

10.0 CABLE

Cable shall be shielded twisted pair approved for EIA-422/EIA-485 use. Examples of suitable cable are:
Belden 9841, Alpha 5271 (one pair, no spares provided), Belden 9842, Alpha 5272 (two pairs, one as a spare)

11.0 MARKING AND IDENTIFICATION

Equipment conforming to this Standard may be marked "USITT DMX512/1990" or DMX512/1990".

Only receivers capable of accepting a 4 μSecond MARK AFTER BREAK may be marked and identified as "USITT DMX512/1990 (4 μSec)" or "DMX512/1990 (4 μSec)".

Compliance with this Standard is the responsibility of the manufacturer and such marking and identification does not constitute certification or approval by the USITT.